METHOD FOR FABRICATING TRANSISTOR GATE STRUCTURES AND GATE DIELECTRICS THEREOF

RELATED APPLICATIONS

5   This application is related to U.S. Patent Application Serial No. 10/185,326, filed on June 28, 2002, entitled ANNEAL SEQUENCE FOR HIGH-K FILM PROPERTY OPTIMIZATION; U.S. Patent Application Serial No. 10/232,124, filed on August 30, 2002, entitled GATE STRUCTURE AND METHOD; and U.S. Patent No. 6,544,906, filed October 25, 2001, entitled

10   ANNEALING OF HIGH-K DIELECTRIC MATERIALS, wherein the entirety of these applications and patents are hereby incorporated by reference as if fully set forth herein.

FIELD OF INVENTION

15   The present invention relates generally to semiconductor devices and more particularly to methods for fabricating and treating high dielectric constant gate dielectrics for MOS transistor-gate structures.

BACKGROUND OF THE INVENTION

20   Field effect transistors (FETs) are widely used in the electronics industry for switching, amplification, filtering, and other tasks related to both analog and digital electrical signals. Most common among these are metal-oxide-semiconductor field-effect transistors (MOSFET or MOS), in which a gate is energized to create an electric field in an underlying channel region of a

25   semiconductor body, by which electrons are allowed to travel through the channel between a source region and a drain region of the semiconductor body. Complementary MOS (CMOS) devices have become widely used in the semiconductor industry, wherein both n-channel and p-channel (NMOS and PMOS) transistors are used to fabricate logic and other circuitry.

30   The source and drain are typically formed by adding dopants to targeted regions of a semiconductor body on either side of the channel. A gate structure

is formed above the channel, having a gate dielectric formed over the channel and a gate electrode above the gate dielectric. The gate dielectric is an insulator material, which prevents large currents from flowing into the channel when a voltage is applied to the gate electrode, while allowing such an applied gate

5 voltage to set up an electric field in the channel region in a controllable manner. Conventional MOS transistors typically include a gate dielectric formed by depositing or growing silicon dioxide (SiO_2) over a silicon wafer surface, with doped polysilicon formed over the SiO_2 to act as the gate electrode.

Continuing trends in semiconductor device manufacturing include

10 reduction in electrical device feature sizes (scaling), as well as improvements in device performance in terms of device switching speed and power consumption. MOS transistor performance may be improved by reducing the distance between the source and the drain regions under the gate electrode of the device, known as the gate or channel length, and by reducing the thickness of the layer of gate

15 oxide that is formed over the semiconductor surface. However, there are electrical and physical limitations on the extent to which thickness of SiO_2 gate dielectrics can be reduced. For example, very thin SiO_2 gate dielectrics are prone to large gate tunneling leakage currents resulting from direct tunneling through the thin gate oxide. In addition, there are conventional limitations on the

20 ability to form such thin oxide films with uniform thickness. Furthermore, thin SiO_2 gate dielectric layers provide a poor diffusion barrier to dopants, for example, and may allow high boron dopant penetration into the underlying channel region of the silicon during fabrication of the source/drain regions.

Recent MOS transistor scaling efforts have accordingly focused on high-k

25 dielectric materials having dielectric constants greater than that of SiO_2 (*e.g.*, greater than about 3.9), which can be formed in a thicker layer than scaled SiO_2, and yet which produce equivalent field effect performance. The relative electrical performance of such high-k dielectric materials is often expressed as equivalent oxide thickness (EOT), because the high-k material layer may be thicker, while

30 still providing the equivalent electrical effect of a much thinner layer of SiO_2. Since the dielectric constant "k" is higher than that of silicon dioxide, a thicker

high-k dielectric layer can be employed to mitigate tunneling leakage currents, while still achieving the equivalent electrical performance of a thinner layer of thermally grown SiO_2, nitrided SiO_2, or SiON.

The performance and reliability of the resulting MOS transistors is dependent upon the quality of the high-k gate dielectric material, including the bulk high-k material and also the quality of the interface region between the high-k gate dielectric material and the underlying silicon. Unlike SiO_2, which may be formed by thermal oxidation (growth process), high-k dielectrics are typically deposited over the semiconductor substrate, using chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), molecular beam epitaxy (MBE), or other deposition processes. While the macroscopic composition (*e.g.*, stoichiometry) of these materials may be controlled to a certain extent during such deposition processes, stoichiometric composition variations within the film may degrade device performance.

In addition, the above deposition techniques often create high-k dielectric films having point defects that affect transistor performance. Such defects may include oxygen vacancies, and/or other point defects affecting leakage through the gate dielectric. Furthermore, certain deposition processes (*e.g.*, CVD, ALD, etc.) may introduce impurities (*e.g.* Cl, C, OH, H, etc.) into the deposited high-k dielectric film, which also degrade device performance. Moreover, the deposited film may not be of optimal density, wherein sub par performance may result. Accordingly, there is a need for improved gate dielectric fabrication techniques by which high quality gate dielectrics and interfaces can be achieved.

SUMMARY OF THE INVENTION

The following presents a simplified summary in order to provide a basic understanding of one or more aspects of the invention. This summary is not an extensive overview of the invention, and is neither intended to identify key or critical elements of the invention, nor to delineate the scope thereof. Rather, the primary purpose of the summary is to present some concepts of the invention in

a simplified form as a prelude to the more detailed description that is presented later.

The invention provides methods for treating deposited high-k gate dielectric films and gate fabrication techniques, by which improved gate dielectric materials may be realized. A deposited dielectric film or layer is subjected to one or more non-oxidizing anneals to densify the material and one or more oxidizing anneals to mitigate material defects. In addition, the film is nitrided to inhibit dopant diffusion and to thermally stabilize the deposited material. The nitridation may be done first, or one or more of the anneals can be performed prior to nitridation to densify and/or heal defects resulting from the initial deposition process. After nitridation, one or more anneals may be performed to address any defects, impurities, etc. introduced during the nitridation, wherein the post-nitridation annealing may be performed at high temperatures without crystallization, due to the presence of nitrogen in the film.

One aspect of the invention combines a post-deposition nitridation process with two or more post-deposition anneal operations, where one is oxidizing and one is non-oxidizing. In accordance with this aspect, a method is provided for treating a deposited high-k gate dielectric layer during fabrication of a semiconductor device. The method comprises nitriding a deposited high-k gate dielectric layer, performing a first anneal in a non-oxidizing ambient, and performing a second anneal in an oxidizing ambient. In one implementation, the nitridation is done prior to both the anneal processes, with the non-oxidizing anneal being done last (e.g., prior to depositing the gate electrode material). In another implementation, the non-oxidizing anneal is done prior to nitridation. Either implementation may be used in conjunction with nitrogen-containing high-k materials or with materials initially deposited with no nitrogen content, wherein the nitridation step may improve thermal stability of the deposited material in either case.

Another aspect of the invention provides a post-deposition nitridation process, along with one or more pre-nitridation anneal processes and one or more post-nitridation anneal processes to treat the high-k material. In one

example, the pre-nitridation anneals include a first anneal at a moderate temperature in a non-oxidizing ambient that operates to densify the deposited high-k material, wherein the temperature of the first anneal may be adjusted to avoid crystallizing the material, particularly important for deposited films initially

5   having no nitrogen content. A second pre-nitridation anneal is then performed at moderate temperatures in an oxidizing ambient to reduce or eliminate defects and impurities in the high-k dielectric before nitridation. The post nitridation annealing in this example includes a third anneal process performed at a high temperature in a non-oxidizing ambient to densify the material, followed by a

10   fourth anneal at a somewhat lower temperature in an oxidizing ambient to control point defects.

The following description and annexed drawings set forth in detail certain illustrative aspects and implementations of the invention. These are indicative of but a few of the various ways in which the principles of the invention may be

15   employed.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a simplified flow diagram illustrating an exemplary method of fabricating transistor gate structures in accordance with the present invention;

20   Fig. 2 is a flow diagram illustrating another exemplary method of fabricating transistor gate structures in accordance with the invention;

Figs. 3A-3I are partial side elevation views in section illustrating a semiconductor device at various stages of fabrication processing wherein a high-k gate dielectric is formed and treated in accordance with the method of Fig. 2;

25   and

Fig. 4 is a flow diagram illustrating another exemplary method of fabricating transistor gate structures in which a deposited high-k gate dielectric material layer undergoes a high temperature non-oxidizing anneal prior to nitridation or undergoes nitridation prior to a high temperature inert non-oxidizing

30   anneal in accordance with the invention.

DETAILED DESCRIPTION OF THE INVENTION

One or more implementations of the present invention will now be described with reference to the attached drawings, wherein like reference numerals are used to refer to like elements throughout, and wherein the devices and structures illustrated in the figures are not necessarily drawn to scale.

The invention relates to post-deposition treatment of deposited high-k gate dielectric films to densify the material, heal defects, and to thermally stabilize the material through multiple anneal processes and a nitridation process. The methods of the invention can be employed following high-k deposition and before formation of gate electrode materials over the high-k, to improve the high-k material quality (*e.g.*, reduce point and other defects, densify the material, remove impurities, etc.). The techniques of the invention may be employed in conjunction with any high-k dielectric materials having a dielectric constant "k" greater than that of SiO_2 (*e.g.*, greater than about 3.9), and are independent of the particular deposition process used to initially form the high-k film. In addition, the invention may be employed in devices fabricated using any semiconductor body (*e.g.*, silicon substrates, SOI wafers, etc.), and may be used in transistors having any type of gate electrode material(s) (*e.g.*, polysilicon, metal gates, etc.).

Referring initially to Fig. 1, a gate fabrication method 10 is hereinafter illustrated and described in accordance with one or more aspects of the present invention. Although the exemplary method 10 and other methods of the invention are illustrated and described below as a series of acts or events, it will be appreciated that the present invention is not limited by the illustrated ordering of such acts or events. For example, some acts may occur in different orders and/or concurrently with other acts or events apart from those illustrated and/or described herein, in accordance with the invention. In addition, not all illustrated steps may be required to implement a methodology in accordance with the present invention. Further, the methods according to the present invention may be implemented in association with the formation and/or processing of structures illustrated and described herein as well as in association with other structures and devices not illustrated.

Beginning at 12, the method 10 comprises depositing a high-k gate dielectric layer at 14. Any dielectric may be deposited at 14 having a dielectric constant higher than that of SiO_2, including but not limited to binary metal oxides including aluminum oxide (Al_2O_3), zirconium oxide (ZrO_2), hafnium oxide (HfO_2),

5 lanthanum oxide (La_2O_3), yttrium oxide (Y_2O_3), titanium oxide (TiO_2), as well as their silicates and aluminates; metal oxynitrides including aluminum oxynitride (AlON), zirconium oxynitride (ZrON), hafnium oxynitride (HfON), lanthanum oxynitride (LaON), yttrium oxynitride (YON), as well as their silicates and aluminates such as ZrSiON, HfSiON, LaSiON, TaSiON, YSiON, ZrAlON,

10 HfAlON, TaAlON, etc.; and perovskite-type oxides including a titanate system material such as barium titanate, strontium titanate, barium strontium titanate (BST), lead titanate, lead zirconate titanate, lead lanthanum zirconate titanate, barium lanthanum titanate, barium zirconium titanate; a niobate or tantalate system material such as lead magnesium niobate, lithium niobate, lithium

15 tantalate, potassium niobate, strontium aluminum tantalate and potassium tantalum niobate; a tungsten-bronze system material such as barium strontium niobate, lead barium niobate, barium titanium niobate; and Bi-layered perovskite system material such as strontium bismuth tantalate, bismuth titanate and others. Furthermore, any deposition process or processes may be employed in

20 depositing the high-k film at 14, including but not limited to CVD, PVD, ALD, MBE, or others.

Following the high-k deposition at 14, a multi-step treatment is performed at 16, including one or more pre-nitridation anneals at 18, a nitridation process at 20, and one or more post-nitridation anneals at 22. As illustrated and described

25 further below with respect to Figs. 2 and 3A-3I, the multi-step treatment 16 may advantageously comprise first and second pre-nitridation anneals at 18, wherein a first anneal is performed at a moderate temperature in an inert non-oxidizing ambient for densifying the deposited high-k material, as well as a second pre-nitridation anneal at 18 that is performed in an oxidizing ambient for curing

30 defects and eliminating impurities. Moreover, the post-nitridation annealing at 22 in the example below advantageously includes a third anneal performed at a high

temperature in a non-oxidizing ambient to densify the thermally stabilized high-k material and a fourth anneal in an oxidizing ambient to reduce any remaining defects and impurities.

At 24, a gate electrode material (*e.g.*, polysilicon, metals, metal silicides, metal oxides, metal nitrides, or stacks combinations thereof) is formed over the treated high-k dielectric, using any suitable deposition process. The gate dielectric and gate electrode material layers are then patterned at 26 (*e.g.*, using suitable etch masks and reactive ion etching (RIE) or other selective material removal processes) to create a patterned gate structure over a prospective channel region of the underlying semiconductor body, and the gate fabrication method 10 ends at 28. Thereafter, further processing steps may be undertaken to complete fabrication of a finished MOS transistor, for example, including implantation of source/drain regions of the substrate (*e.g.*, as well as implantation of a polysilicon gate electrode material), silicidation to form contacts over the gate and the source/drains, and metalization or interconnect processing (not shown).

Referring now to Figs. 2 and 3A-3I, an exemplary implementation of the invention is illustrated and described in the context of treating a deposited high-k dielectric prior to formation of a gate electrode material thereover. Fig. 2 illustrates a gate fabrication method 50 and Figs. 3A-3I illustrate an exemplary semiconductor device 102 undergoing gate fabrication processing generally in accordance with the method 50. Beginning at 52 in Fig. 2, a high-k dielectric (*e.g.*, such as those described above) is deposited or otherwise formed at 54 over or above a semiconductor body. In one example, HfSiO or HfSiON may be deposited over a silicon substrate at 54 *via* CVD, PVD, ALD, PECVD, PEALD, MBE, or other suitable deposition process.

In Fig. 3A, the exemplary device 102 is illustrated after shallow trench isolation (STI) or field oxide (LOCOS) isolation structures 112 and one or more wells 118 have been formed in a silicon wafer substrate 104. A pre-deposition cleaning operation 116 is performed in Fig. 3A. In Fig. 3B, a CVD process 122 is used to deposit a HfSiO high-k dielectric layer 120 at a deposition temperature

below about 700 degrees C. It is noted in this example, that other high-k materials may be deposited at 54 in the method 50, including those having nitrogen content (e.g., HfSiON, etc.). As noted above, the deposited high-k layer may include stoichiometric composition variations, defects that affect transistor performance (e.g., oxygen vacancies, and/or other point defects that may lead to gate dielectric leakage and/or interface states). In this regard, the deposition process at 54 may itself introduce impurities into the deposited high-k dielectric film, which also degrade device performance. For example, CVD or ALD deposited HfSiO may include undesirable C, OH, H, Cl, or other impurities, wherein ALD deposition is typically at a lower temperature (e.g., about 300 degrees C) and the corresponding presence of C, OH, or Cl impurities is higher.

As discussed above, the optimization of the high-k dielectric film properties with respect to transistor performance is facilitated by film densification, nitrogen incorporation, and defect/impurity reduction through oxidation, wherein nitrogen incorporation may be preceded by densification. In addition, defect/impurity reduction can be facilitated by high temperature annealing, where nitrogen incorporation (e.g., thermal stabilization) facilitates the use of higher annealing temperatures without crystallizing the deposited high-k material. Low temperature oxidizing anneals avoid increases in the EOT of the material, but generally do not densify the material. At the same time, non-oxidizing high temperature anneals (e.g., Ar, He, or N_2 ambient) facilitate densification, but typically do not heal defects or adjust for non-stoichiometry.

It is noted with respect to HfSiO and HfSiON that while initially including nitrogen in the high-k material as deposited facilitates higher temperature annealing, HfSiO has been found to be easier to deposit at 54 than HfSiON. The same may be true of other non-nitrogen containing deposited high-k materials. Moreover, the introduction of further nitrogen into materials that initially contained nitrogen (e.g., HfSiON as deposited) is believed to benefit the high-k film properties and the resulting device performance. In this regard, a post-deposition nitridation can be used to fine tune the nitrogen content and profile

throughout the depth of the high-k film, for example, with little or no nitrogen at the interface between the substrate and the high-k material.

Accordingly, to address these interrelationships between deposition processing, annealing, nitrogen incorporation, densification, defect/impurity reduction, etc., the exemplary method 50 includes a nitridation at 70, as well as pre and post nitridation annealing at 60 and 80, respectively, to reduce defects/impurities, densify the high-k material, and incorporate nitrogen therein, without creating unwanted low-k oxidation at the dielectric/substrate interface. In general, deposited materials that include nitrogen content (as deposited) may be annealed at somewhat higher temperatures at 60, wherein the pre and post-nitridation anneal temperatures can be tailored to prevent crystallization of the high-k material. For example, deposited HfSiO has been found to crystallize at about 900 degrees C, whereas HfSiON may be stable above about 1100 degrees C, depending on the composition (Hf to Si ratio and N to O ratio). The same general relationships are believed to be true for other high-k dielectrics, where nitrogen incorporation at 54 increases the thermal stability allowing higher anneal temperatures at 60, wherein such thermal stability considerations may be taken into account in determining both the pre and post nitridation anneal temperatures at 60 and 80, respectively.

At 60, pre-nitridation annealing of the high-k material is performed to address densification, defects, and impurity issues that may have arisen during the deposition at 54. A dual anneal sequence is employed at 60, including an inert anneal at 62 and an oxidizing anneal at 64. Suitable first and second anneal processes are described in U.S. Patent Application No. 10/185,326, assigned to the assignee of the present invention Texas Instruments Incorporated, the entirety of which is hereby incorporated by reference as if fully set forth herein. In the exemplary method 50, a first (pre-nitridation) anneal is performed at a moderate temperature at 62 in an inert non-oxidizing ambient, in order to initially densify the deposited high-k material.

As illustrated in Fig. 3C, the device 102 undergoes a first anneal process 124 to densify the high-k material 120. The first anneal 124 occurs in a non-

oxidizing ambient, for example, comprising Ar, He, or N_2 at a relatively high or moderate temperature, preferably in the range of 700° C to 1100° C, for about 60 seconds in one example to densify the high-k gate dielectric 120. In the illustrated example of deposited HfSiO or HfSiON, the first anneal 124 (62 in Fig.

5   3) is performed at a temperature of about 1000 degrees C or less (*e.g.*, deposited HfSiON), preferably about 900 degrees C or less (*e.g.*, deposited HfSiO), such as about 700 to 900 degrees C, in a non-oxidizing ambient comprising N_2, Ar, He, Ne, or other inert gas environment. In this example, the first anneal at 62 operates to completely or partially densify the deposited high-k

10   material wherein applying thermal energy allows the deposited atoms to slightly rearrange themselves into more stable positions, leaving fewer dangling bonds in a higher density material, without excessive atomic rearrangement (*e.g.*, without crystallization or phase separation). This, in turn, leads to fewer interface states and lower dielectric leakage in the finished MOS transistor device 102.

15   Referring also to Fig. 3D, a second anneal is performed at 64 (anneal process 126 in Fig. 3D), wherein an oxidizing ambient is used to heal oxygen defects, and to eliminate or reduce carbon, hydrogen, chlorine, or other impurities. In one implementation, the second anneal at 64 is performed at a temperature of about 1000 degrees C or less, preferably about 700 degrees C or

20   less, at atmospheric pressure, preferably at a pressure of about 1 Torr or less. This second anneal at 64, moreover, can be any form of relatively mild anneal in an oxidizing ambient to heal the film and interface defects incurred during the deposition at 54. The oxidizing ambient may comprise, for example, O_2, N_2O, NO, ozone (O_3), UV O_2, or other suitable oxidizing ambient. The second anneal

25   is a preferably performed at 64 at a lower temperature than the first anneal at 62 (*e.g.*, room temperature to 1000° C), and may be a thermal anneal, with or without UV exposure, or a low temperature plasma process, wherein the process temperature, time and pressure may be selected so as not to significantly increase the material EOT. In this regard, reduced pressure may be helpful in

30   avoiding oxide growth (increased EOT), wherein reduced pressures may allow higher temperatures during the second anneal at 64.

For example, the second anneal may be performed at about 700 degrees C in an O_2 ambient for about 60 sec at 1 Torr. The first and second anneals at 60, as well as the nitridation 70 and/or the post-nitridation anneals at 80 may be separate processes or may be run as separate steps within one recipe. For example, depending on the anneal tool configuration, the dual pre-nitridation anneals at 60 may be performed in a single processing run with a multi-step annealing recipe. The second anneal at 64 may alternatively comprise exposing the high-k dielectric layer to an oxidizing liquid solution, such as $H_2O + H_2O_2$, $H_2O + O_3$, $H_2SO_4 + H_2O_2 + H_2O$, $H_2SO_4 + H_2O$, $HNO_3 + H_2O$, $HNO_3 + H_2O_2 + H_2O$, $HCl + H_2O_2 + H_2O$, or $NH_4OH + H_2O_2 + H_2O$. Suitable liquid based oxidation surface treatments are set forth in U.S. Patent Application No. 10,232,124, filed on August 30, 2002, assigned to the assignee of the present invention Texas Instruments Incorporated, the entirety of which is hereby incorporated by reference as if fully set forth herein.

In another alternative, the second anneal at 64 may comprise an oxidizing plasma process at 700 degrees or less (e.g., low temperature oxidizing plasma process). In this case, the high-k material 120 is exposed to an oxygen plasma in an ambient including, for example, O_2 with one or more of Ar, N_2O or NO, where the plasma provides energized oxygen ions to the high-k material 120. In another possible implementation, the second anneal at 64 can be an ozone anneal, wherein the process ambient includes O_3. In still another possibility, the second anneal can be a low temperature anneal (e.g., less than about 700 degrees C) with UV excitation, for example, wherein O_2 gas is energized with UV lamps to create atomic oxygen or O_3 that are provided to the high-k material 120.

Thereafter at 70, a plasma nitridation process is performed (process 128 in Fig. 3E) to introduce nitrogen into the high-k material 120. The plasma nitridation at 70 may be performed according to any suitable process parameters. One possible implementation is described in U.S. Patent No. 6,136,654, issued 10/24/00 to Kraft et al., assigned to the assignee of the present invention Texas Instruments Incorporated, the entirety of which is hereby incorporated by reference as if fully set forth herein. In two possible implementations, the

nitridation at 70 may comprise a nitridation anneal, for example, in an NH_3 (e.g., ammonia) ambient, or a plasma nitridation process. In the case of an ammonia anneal, the nitridation at 70 may be performed in the same process tool used for the pre and/or post anneals at 60 and 80.

5   The introduction of nitrogen can be used to block boron diffusion, thermally stabilize the film (e.g., raise the temperature of crystallization or phase separation), and to increase the dielectric constant k. For example, for deposited HfSiO, the nitridation at 70 creates HfSiON, which may be thermally stable above about 1100 degrees C without crystallizing. Where the deposited film 120

10   already includes nitrogen, the nitridation 70 can be employed to tune the nitrogen content/profile through the depth of the film. In order to avoid having nitrogen at the interface, this nitridation step 70 can be advantageously employed, for example, to introduce nitrogen primarily near the top of the film 120. In the case of an ammonia (NH_3) anneal, the nitridation temperature may be about 1000

15   degrees C or less. Plasma nitridation can alternatively be employed at 70, for example, including performing a decoupled-plasma-nitridation (DPN) or slot-plane-antenna (SPA) plasma nitridation process.

      The inventors have appreciated that although the pre-nitridation anneals at 60 facilitate defect/impurity reduction and densification, some

20   defects/impurities may remain prior to the nitridation at 70. Furthermore, the nitridation at 70 itself may cause defects and/or introduce impurities in the high-k dielectric 120. For instance, an ammonia anneal at 70 can introduce H into the film 120, and may also renitride the substrate/high-k interface slightly. For a plasma nitridation at 70, the incoming nitrogen atoms are energized, and can

25   knock oxygen out of the film 120, thereby creating new oxygen vacancies. Thus, the nitridation at 70 can recreate some of the defects that the pre-nitridation anneal 60 was meant to cure.

      Accordingly, the method 50 further comprises one or more post-nitridation anneals at 80. The post-nitridation anneals densify the material 120 through inert

30   annealing at high temperature, and reoxidize the material 120, wherein the reoxidation operates to heal defects caused by the nitridation 70, eliminate

hydrogen, potentially regrow the interface to inhibit interface nitridation between the substrate 104 and the high-k material 120, and to fix oxygen vacancies in the film 120. In the exemplary method 50, the post-nitridation anneals 80 include a high temperature inert anneal at 82 to densify the film through slight atomic

5 rearrangement without crystallization (third anneal process 130 in Fig. 3F). This third anneal at 82 can be greater than about 1000 degrees C in an inert ambient (e.g., comprising N_2, Ar, He, or Ne) for HfSiON or other high-k materials 120 due to the thermal stabilization afforded by the nitridation at 70. Alternatively, any other suitable non-oxidizing anneal can be used at 82 that does not drastically

10 change the film composition profile (e.g., below the crystallization temperature).

At 84, a fourth anneal is performed (e.g., anneal process 132 in Fig. 3G) at a mild temperature in an oxidizing ambient to fix the high-k material composition and heal any remaining defects in the film 120. The fourth anneal at 84 is preferably performed at a temperature of about 1000 degrees C or less, for

15 example, about 700 degrees C or less, and at a pressure of about 1 Torr or less in one example, or at atmospheric pressure in another example. As with the second anneal at 64, the fourth anneal may be any suitable oxidizing anneal process, such as exposing the high-k dielectric layer to an oxidizing liquid solution (e.g., $H_2O + H_2O_2$, $H_2O + O_3$, $H_2SO_4 + H_2O_2 + H_2O$, $H_2SO_4 + H_2O$, HNO_3

20 $+ H_2O$, $HNO_3 + H_2O_2 + H_2O$, $HCl + H_2O_2 + H_2O$, $NH_4OH + H_2O_2 + H_2O$, etc.), an oxidizing plasma process, an ozone anneal, a low temperature anneal with UV excitation, etc.

One, some or all of the anneals 60, 80, and the nitridation 70 may be performed in a single process tool, for example, where the nitridation at 70 is an

25 NH_3 anneal. Thereafter at 90, polysilicon gate electrode material is formed over the high-k dielectric 120 (e.g., polysilicon layer 140 deposited via a deposition process 142 in Fig. 3H). At 92, the gate dielectric and gate electrode material layers are patterned to create a patterned gate structure over a prospective channel region of the underlying semiconductor body, and the gate fabrication

30 method 50 ends at 94. Further processing is then performed as illustrated in Fig. 3I to implant source/drain regions 150 in the substrate 104 and to form sidewall

spacers 160 along the lateral sides of the patterned gate structure. Silicidation and metalization processing is thereafter performed (not shown) to complete the fabrication of the device 102.

Referring now to Fig. 4, another aspect of the invention provides for dual high-k gate dielectric annealing (an oxidizing anneal and a non-oxidizing anneal) with material nitridation, wherein these three processes may be performed in any order following the high-k deposition and before formation of an overlying gate electrode material. Fig. 4 illustrates another method 200 for gate fabrication in accordance with this aspect of the invention, beginning at 202, wherein the nitridation may be performed prior to both anneals or between two anneals. A high-k gate dielectric material layer is deposited at 204, which may form any high-k material such as those described above *via* any suitable deposition process (*e.g.*, CVD, PVD, ALD, MBE, etc.).

Thereafter, a three step treatment is performed at 210, including a nitridation, an oxidizing anneal, and a non-oxidizing anneal. In one implementation, the method 200 proceeds to 212, where a first anneal is performed in a non-oxidizing ambient at relatively high temperature. The first anneal temperature is selected to densify the high-k material without crystallization. Where the high-k material is initially deposited to include nitrogen, the first anneal temperature at 212 can be higher than for material not initially deposited with nitrogen. For example, where HfSiO is deposited at 204, the first anneal at 212 is preferably performed at a temperature of about 1000 degrees C or less, more preferably at about 700 to 900 degrees C in an inert ambient (*e.g.*, N_2, Ar, He, or Ne) to reduce the likelihood of crystallization. For HfSiON deposited at 204, the non-oxidizing first anneal at 212 may be performed at temperatures up to about 1100 degrees C.

At 214, the densified high-k material is nitrided using any suitable nitridation process, such as those described above. In one example, the nitridation at 214 comprises performing a nitridation anneal in a nitrogen containing ambient, such as annealing at about 1000 degrees C or less in an

TI-35227   15

ammonia (NH_3) ambient. In another possible implementation, the nitridation at 212 is a plasma nitridation process (*e.g.*, SPA, DPN, etc.).

Thereafter at 220, a second anneal is performed in an oxidizing ambient to heal oxygen defects, and to eliminate or reduce carbon, hydrogen, chlorine, or other impurities, including those associated with the deposition process at 204 as well as those associated with the nitridation at 214. In one implementation, the second anneal at 220 is performed at a temperature of about 1000 degrees C or less, preferably about 700 degrees C or less, at atmospheric pressure or a pressure of about 1 Torr or less. The oxidizing ambient may comprise, for example, O_2, N_2O, NO, ozone (O_3), UV O_2, or other suitable oxidizing ambient. The second anneal at 220, moreover, may be a thermal anneal, with or without UV exposure, or a low temperature oxidizing plasma process, wherein the process temperature, time and pressure may be selected so as not to significantly increase the material EOT, such as the oxidizing anneals described above. In another example, the second anneal at 220 may comprise exposing the high-k dielectric layer to an oxidizing liquid solution, such as $H_2O + H_2O_2$, $H_2O + O_3$, $H_2SO_4 + H_2O_2 + H_2O$, $H_2SO_4 + H_2O$, $HNO_3 + H_2O$, $HNO_3 + H_2O_2 + H_2O$, $HCl + H_2O_2 + H_2O$, or $NH_4OH + H_2O_2 + H_2O$, as described above.

Following the second anneal at 220, a gate electrode material (*e.g.*, polysilicon, etc.) is deposited at 222 over the treated high-k dielectric, using any suitable deposition process. At 224, the treated high-k gate dielectric and gate electrode material layers are patterned to provide a patterned gate structure over the semiconductor body, and the gate fabrication method 200 ends at 226. It is noted in this example, that the first anneal at 212 may need to be performed at a moderate temperature, particularly for non-nitrogen containing materials deposited at 204, since the nitridation (*e.g.*, thermal stabilization) at 214 is after the first anneal at 212. However, it is further noted that the nitridation 214 itself may be facilitated by densification of the high-k material through annealing at 212, which may improve tailoring of the nitrogen content and profile in the high-k material.

In another exemplary implementation of the method 200, the post-deposition nitridation is performed prior to both of the anneal processes. After the high-k deposition at 204, the method 200 proceeds to 216, where the high-k material is nitrided using any suitable nitridation process (*e.g.*, a nitridation

5   anneal in a nitrogen containing ambient, SPA or DPN plasma nitridation, etc., as described above). In this example, the high-k material has not been densified at the time of the nitridation 216, but the nitridation at 216 may advantageously allow higher temperature densification annealing by thermally stabilizing the material prior to the densification (*e.g.*, non-oxidizing) anneal at 218.

10   After the nitridation at 216, the method proceeds to 218, where a first anneal is performed in a non-oxidizing ambient to densify the material. The first anneal can be performed according to any of the non-oxidizing anneal examples set forth above, wherein the annealing temperature may be relatively high because the high-k material has been thermally stabilized by the nitridation at

15   216. In this example, the incorporation of nitrogen at 216 may proceed at a higher rate in the non-densified material than for the above case where the material is first densified (*e.g.*, 212 and 214 in Fig. 4), which may be advantageous for non-nitrogen containing deposited films. Thereafter, the method 200 proceeds to the second (*e.g.*, oxidizing) anneal 220, electrode

20   deposition 222 and patterning at 224 as described above, before the method 200 ends at 226.

Although the invention has been illustrated and described with respect to one or more implementations, alterations and/or modifications may be made to the illustrated examples without departing from the spirit and scope of the

25   appended claims. In particular regard to the various functions performed by the above described components or structures (assemblies, devices, circuits, systems, etc.), the terms (including a reference to a "means") used to describe such components are intended to correspond, unless otherwise indicated, to any component or structure which performs the specified function of the described

30   component (e.g., that is functionally equivalent), even though not structurally equivalent to the disclosed structure which performs the function in the herein

illustrated exemplary implementations of the invention. In addition, while a particular feature of the invention may have been disclosed with respect to only one of several implementations, such feature may be combined with one or more other features of the other implementations as may be desired and

5   advantageous for any given or particular application. Furthermore, to the extent that the terms "including", "includes", "having", "has", "with", or variants thereof are used in either the detailed description and the claims, such terms are intended to be inclusive in a manner similar to the term "comprising".